What is claimed is:

1. A package for an integrated circuit, comprising:

a plurality of layers sealably connectable to each other to form a package having a cavity sized and shaped to receive the integrated circuit, each layer being formed of a respective material, each respective material being suitable for use as a printed circuit board substrate,

at least one of the plurality of layers being a substrate having contacts that are connectable to electrical contacts of the integrated circuit, and

a bottom one of the layers having a plurality of ball attach pads, electrically connected to the contacts of the substrate.

2. The package of claim 1, wherein one of the layers is a superstrate above the substrate, the superstrate having a sufficiently high dielectric constant to provide isolation between a plurality of signal traces on the substrate.

3. The package of claim 2, wherein the superstrate is formed of the same material as the substrate.

4. The package of claim 3, wherein the substrate and superstrate are formed of material comprising PTFE with a ceramic filler.

5. The package of claim 1, wherein the plurality of layers includes at least 5 layers.

6. The package of claim 1, wherein a top one of the plurality of layers is sufficiently rigid to maintain planarity of the package.

7. The package of claim 6, wherein the top layer is formed of FR4 epoxy glass laminate.

8. The package of claim 1, wherein the bottom layer is formed of a glass reinforced hydrocarbon/ceramic laminate.

9. The package of claim 8, wherein a layer formed below the substrate comprises a glass reinforced hydrocarbon/ceramic laminate having an opening sized and shaped to accommodate a chip carrier on which the integrated circuit is mounted.

10. The package of claim 1, wherein the contacts of the substrate are arranged to accommodate a flip-chip mounting of the integrated circuit.

11. An integrated circuit package assembly, comprising:

an integrated circuit; and

a plurality of layers sealably connectable to each other to form a package having a cavity sized and shaped to receive the integrated circuit, each layer being formed of a respective material, each respective material being suitable for use as a printed circuit board substrate,

at least one of the plurality of layers being a substrate having contacts that are connectable to electrical contacts of the integrated circuit, and

a bottom one of the layers having a plurality of ball attach pads, electrically connected to the contacts of the substrate.

12. The package assembly of claim 11, wherein one of the layers is a superstrate above the substrate, the superstrate having a sufficiently high dielectric constant to provide isolation between a plurality of signal traces on the substrate.

13. The pacakge assembly of claim 12, wherein the superstrate is formed of the same material as the substrate.

14. The package assembly of claim 13, wherein the substrate and superstrate are formed of material comprising PTFE with a ceramic filler.

15. The package assembly of claim 11, wherein a top one of the plurality of layers is formed of FR4 epoxy glass laminate.

16. The package assembly of claim 11, wherein the bottom layer is formed of a glass reinforced hydrocarbon/ceramic laminate.

17. A printed circuit board assembly, comprising:

a printed circuit board having a circuit board substrate with circuit traces and a plurality of devices thereon, said plurality of devices including at least one integrated circuit package assembly that includes:

an integrated circuit; and

a plurality of layers sealably connectable to each other to form a package having a cavity sized and shaped to receive the integrated circuit, each layer being formed of a respective material, each respective material being of a type suitable for use in the circuit board substrate,

at least one of the plurality of layers being a package substrate having contacts that are connectable to electrical contacts of the integrated circuit, and

a bottom one of the layers having a plurality of ball attach pads, electrically connected to contacts of the circuit board substrate.

18. The printed circuit board assembly of claim 17, wherein at least one of the plurality of layers is formed from the same material as the printed circuit board substrate.

19. A method of making a package for an integrated circuit, comprising the steps of:

(a) providing a plurality of layers, each formed of a respective material suitable for use as a printed circuit board substrate, at least one of the plurality of layers being a substrate having contacts that are connectable to electrical contacts of the integrated circuit, and

(b) sealably connecting the plurality of layers to each other to form a package having a cavity sized and shaped to receive the integrated circuit, wherein a bottom one of the layers has a plurality of ball attach pads that are electrically connected to the contacts of the substrate.

20. The method of claim 19, wherein step (a) includes providing a superstrate above the substrate, the superstrate having a sufficiently high dielectric constant to provide isolation between a plurality of signal traces on the substrate.

21. The method of claim 20, wherein the superstrate is formed of the same material as the substrate.

22. The method of claim 21, wherein the substrate and superstrate are formed of material comprising PTFE with a ceramic filler.

23. The method of claim 19, wherein the plurality of layers includes at least 5 layers.

24. The method of claim 19, wherein a top one of the plurality of layers is sufficiently rigid to maintain planarity of the package.

25. The method of claim 24, wherein the top layer is formed of FR4 epoxy glass laminate.

26. The method of claim 19, wherein the bottom layer is formed of a glass reinforced hydrocarbon/ceramic laminate.

27. The method of claim 26, wherein a layer formed below the substrate comprises a glass reinforced hydrocarbon/ceramic laminate having an opening sized and shaped to accommodate a chip carrier on which the integrated circuit is mounted.

28. The method of claim 19, wherein the contacts of the substrate are arranged to accommodate a flip-chip mounting of the integrated circuit.